AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor device comprising:

(a) a substrate having a surface;

(b) a dielectric formed over the surface of the substrate; and

(c) a wiring line buried in the dielectric;

the wiring line including a Cu-based conductor and a first cover layer covering an outer surface of the conductor;

the first cover layer being made of refractory metal nitride;

further comprising a second cover layer provided between the conductor and the first cover layer and a third cover layer provided between the conductor and the first cover layer~~;~~, wherein:

the second cover layer covers partially or entirely the outer surface of the conductor, the second cover layer being made of refractory metal;

~~and wherein~~ the third cover layer covers entirely or partially the outer surface of the conductor, the third cover layer being made of dielectric; and

the first cover layer covers at least a portion of a top surface of the conductor.

2. (Original) The device according to claim 1, wherein the first cover layer is made of nitride of at least one selected from the group consisting of titanium (Ti), tantalum (Ta), and tungsten (W).

3. (Cancelled)

4. (Currently Amended) A semiconductor device comprising:

(a) a substrate having a surface;

(b) a dielectric formed over the surface of the substrate; and

(c) a wiring line buried in the dielectric;

the wiring line including a Cu-based conductor and a first cover layer covering an outer surface of the conductor;

the first cover layer being made of refractory metal nitride;

further comprising a third cover layer provided between the conductor and the first cover layer~~,~~ wherein:

the third cover layer covers entirely or partially the outer surface of the conductor, the third cover layer being made of dielectric; and

the first cover layer covers at least a portion of a top surface of the conductor.

5. (Original) The device according to claim 4, wherein the third cover layer covers the outer surface of the conductor at its each side.

6. (Cancelled)

7. (Original) The device according to claim 1, wherein the dielectric formed over the surface of the substrate is made of inorganic material and has a relative dielectric constant ranging from 1.6 to 9.

8. (Original) The device according to claim 1, wherein the dielectric formed over the surface of the substrate is made of organic material and has a relative dielectric constant of 1.6 to 3.

9. (Original) The device according to claim 1, wherein the wiring line has a damascene structure.

10. (Previously Presented) The device according to claim 1, wherein the dielectric in which the wiring line is buried has a composite structure comprising a first dielectric layer, an etch stop layer formed on the first dielectric layer, and a second dielectric layer formed on the etch stop layer;

and wherein a bottom surface of the first cover layer is approximately in a same level as an upper surface of the first dielectric layer;

and wherein a top surface of the first cover layer is approximately in a same level as an upper surface of the second dielectric layer.

11. (Previously Presented) The device according to claim 1, wherein the wiring line buried in the dielectric fills a trench having inner side faces tilted at an angle of 70° to 80° with respect to an imaginary plane of a bottom of the trench.

12. through 24. (Cancelled)

25. (Previously Presented) The device according to claim 1, wherein the first cover layer entirely covers the outer surface of the conductor.

26. (Previously Presented) The device according to claim 4, wherein the first cover layer is made of nitride of at least one selected from the group consisting of titanium (Ti), tantalum (Ta), and tungsten (W)

27. (Previously Presented) The device according to claim 4, further comprising a second cover layer provided between the conductor and the first cover layer;

wherein the second cover layer covers partially or entirely the outer surface of the conductor, the second cover layer being made of refractory metal.

28. (Previously Presented) The device according to claim 4, wherein the dielectric formed over the surface of the substrate is made of inorganic material and has a relative dielectric constant ranging from 1.6 to 9.

29. (Previously Presented) The device according to claim 4, wherein the dielectric formed over the surface of the substrate is made of organic material and has a relative dielectric constant of 1.6 to 3.

30. (Previously Presented) The device according to claim 4, wherein the wiring line has a damascene structure.

31. (Previously Presented) The device according to claim 4, wherein the dielectric in which the wiring line is buried has a composite structure comprising a first dielectric layer, an etch stop layer formed on the first dielectric layer, and a second dielectric layer formed on the etch stop layer;

and wherein a bottom surface of the first cover layer is approximately in a same level as an upper surface of the first dielectric layer;

and wherein a top surface of the first cover layer is approximately in a same level as an upper surface of the second dielectric layer.

32. (Previously Presented) The device according to claim 4, wherein the wiring line buried in the dielectric fills a trench having inner side faces tilted at an angle of 70° to 80° with respect to an imaginary plane of a bottom of the trench.

33. (Previously Presented) The device according to claim 4, wherein the first cover layer entirely covers the outer surface of the conductor.

34. (New) A semiconductor device comprising:

(a) a substrate having a surface;

(b) a dielectric formed over the surface of the substrate; and

(c) a wiring line buried in the dielectric;

the wiring line including a Cu-based conductor and a first cover layer covering an outer surface of the conductor;

the first cover layer being made of refractory metal nitride;

further comprising a second cover layer provided between the conductor and the first cover layer and a third cover layer provided between the conductor and the first cover layer; wherein:

the second cover layer covers partially or entirely the outer surface of the conductor, the second cover layer being made of refractory metal;

the third cover layer covers entirely or partially the outer surface of the conductor, the third cover layer being made of dielectric;

the dielectric in which the wiring line is buried has a composite structure comprising a first dielectric layer, an etch stop layer formed on the first dielectric layer, and a second dielectric layer formed on the etch stop layer;

a bottom surface of the first cover layer is approximately in a same level as an upper surface of the first dielectric layer; and

a top surface of the first cover layer is approximately in a same level as an upper surface of the second dielectric layer.

35. (New) A semiconductor device comprising:

(a) a substrate having a surface;

(b) a dielectric formed over the surface of the substrate; and

(c) a wiring line buried in the dielectric;

the wiring line including a Cu-based conductor and a first cover layer covering an outer surface of the conductor;

the first cover layer being made of refractory metal nitride;

further comprising a third cover layer provided between the conductor and the first cover layer; wherein:

the third cover layer covers entirely or partially the outer surface of the conductor, the third cover layer being made of dielectric;

the dielectric in which the wiring line is buried has a composite structure comprising a first dielectric layer, an etch stop layer formed on the first dielectric layer, and a second dielectric layer formed on the etch stop layer;

a bottom surface of the first cover layer is approximately in a same level as an upper surface of the first dielectric layer; and

a top surface of the first cover layer is approximately in a same level as an upper surface of the second dielectric layer.